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10/743,104	12/23/2003	Mitsuhiko Ogihara	MAE 305	8001

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
3663	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/743,104	OGIHARA ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/07/05*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-6,9,10,16-20 and 26-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-6,16-20 and 26-34* is/are rejected.

7)☒ Claim(s) *9,10 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 12/07/05 forms the basis for this office action. Comments on Remarks are included below under "Response to Arguments".

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. ***Claims 2, 4, 5, 17, 19 and 29*** are rejected under 35 U.S.C. 102(b) as being anticipated by Zhang et al (6,255,705 B1).

On claim 5: Zhang et al teach a combined semiconductor apparatus (see Figures 1E and 3B, and columns 7-16) comprising: a semiconductor substrate 101 (col. 11, l. 62-65) having an integrated circuit (CMOS circuit comprising transistors 151 and 152; Figure 1E and col. 8, l. 1-3); a planar region (upper surface-oxidized surface of single-crystal silicon substrate 101) in the surface of 101 underneath transistor 150 is planar as evidenced from Figure 1E) formed in a surface of said semiconductor substrate; a semiconductor thin film (crystalline silicon film 125/126/127 resulting from 104) (col. 12, l. 3-8 and col. 8, l. 22-26) including at least one semiconductor device (namely the active region 126 of TFT 153; see Figure 1E and col. 7, l. 60-67) and bonded on said planar region (through said a planar film 102 (col. 11, l. 65 – col. 12, l. 9); and a planar film 102 disposed between said planar region (upper oxidized surface of semiconductor substrate 101) and said semiconductor thin film (125/126/127 resulting from 104) (see

Figure 1E), said planar region being planar on the side of the semiconductor device (see Figure 1E).

The limitation "planarized" only has patentable weight in the device application of applicant to the extent the final structure is further limited by it. But the limitation "planarized" in "planarized region" and in "planarized film" (lines 4 and 7) does not carry patentable weight for the final structure, because whether a planarization step was carried out in an attempt to make a structure planar is only a limitation on the method of making said structure, and as such even only guarantees an attempt has been made to make said structure or layer planar.

Similarly, the limitation "wherein a surface of said planarized film on a side of said semiconductor thin film has been subjected to a planarizing process" does not further limit said planarized, i.e., planar, film so long as the planar surface of said planar film is on the side of the semiconductor device, which, as we have seen, is the case.

In conclusion, Zhang et al anticipate claim 5.

On claim 2: said planar region is a part of said surface of said semiconductor substrate (upper surface-oxidized surface of single-crystal silicon substrate 101). Again: whether a planarizing process has been carried out has no patentable weight in the present device invention, with reference to the discussion on this topic in the rejection of claim 5.

On claim 4: said planarized region is disposed in a region of said semiconductor substrate adjacent to (i.e., nearby) said integrated circuit of said semiconductor

substrate because TFTs 151, 152 are adjacent to TFT 153, being provided on the same substrate.

On claim 17: said at least one semiconductor apparatus is a light-emitting element (active matrix LCD) (col. 7, l. 49-44) and said integrated circuit 151/152 includes a driving-IC driving said at least one semiconductor device (col. 7, l. 48-52).

On claim 19: in Zhang et al said semiconductor device is a single semiconductor device (active layer of pixel TFT 153) disposed in said semiconductor thin film.

On claim 29: a first surface of said semiconductor thin film, in which said semiconductor device is formed, is disposed on a side of said semiconductor substrate, namely: the upper main side (see Figure 1E).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 3, 6, 18, 26 and 30-31*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al as applied to claim 5, in view of Walker et al (6,841,813 B2).

On claim 6: As detailed above, Zhang et al anticipate claim 5. Zhang et al do not necessarily teach the further limitations defined by claim 6.

However, it would have been obvious to include said limitations *in view of Walker et al, who*, in a patent on integrated devices including TFTs (col. 1), hence analogous art,

teach the stacking of TFT devices in three-dimensional arrays including a plurality of different vertical planar device levels 3A and 3B (abstract and Figures 1 and 4) (col. 4, l. 30-39 and col. 6, l. 47-53); see also first and second planar layers 26 and 27 (col. 5, l. 55-65) in Figure 5A. Because the planarized film of the claim can be identified with any of the interlayer insulation films other than at the vertically highest level, e.g., with 3B, the claim limitation is met through the inclusion of the teaching by Walker et al of three-dimensional TFT mask ROM array with said planar layers, because planar film 3B is disposed between the planarized region formed by the upper main surface of the substrate and the semiconductor thin film of the TFT overlying said planar film 3B while 3B includes an electrically conductive layer, namely the gate layer of any of the TFTs in 3B, and 3B also includes an interlayer dielectric layer formed in a region peripheral, i.e., surrounding, said gate layer, namely the remainder of 3B (Figure 4B, e.g.). *Motivation* to include the teaching by Walker et al is their teaching of the reduction of the effective cell array through their three-dimensional array (col. 3, l. 3-10).

On claim 3: the above-described incorporation of the teaching by Walker et al implies a planar region disposed above an integrated circuit (any circuit integrated in the device on said semiconductor substrate that is located at a lower level than a planar region in a surface of one of the semiconductor channel layers 13 (Figure 3 and col. 5, l. 42) positioned at a level that is higher than said lower level).

On claim 18: in the combined invention according to Zhang et al with three-dimensional array levels implemented according to Walker et al a plurality of

semiconductor devices are arranged in said semiconductor thin film 13 (see Figure 5A and col. 5, l. 41-43, for instance).

On claim 26: Zhang et al teach a combined semiconductor apparatus (see Figures 1E and 3B, and columns 7-16) comprising:

a semiconductor substrate 101 (col. 11, l. 62-65) having an integrated circuit (circuit comprising transistors 151 and 152; Figure 1E);

a planar region (upper surface-oxidized surface of single-crystal silicon substrate 101) in the surface of 101 underneath transistor 150 is planar as evidenced from Figure 1E) formed in a surface of said semiconductor substrate;

a semiconductor thin film (crystalline silicon film 125/126/127 resulting from 104) (col. 12, l. 3-8 and col. 8, l. 22-26) including at least one semiconductor device (namely the active region 126 of TFT 153; see Figure 1E and col. 7, l. 60-67) and bonded on said planar region (through said a planar film 102 (col. 11, l. 65 – col. 12, l. 9); and

an integrated circuit (circuit with transistors 151 and 152) (col. 7, l. 37-60) disposed on said semiconductor substrate 101 (see Figure 1E).

Zhang et al do not necessarily teach the further limitations on "a raised layer" and "another semiconductor film" as defined by the final 6 lines of claim 26. *However, it would have been obvious to include said further limitation in view of Walker et al,* who, in a patent on integrated devices including TFTs (col. 1), hence analogous art, teach, so as to decrease cost through reduction of effective cell area by means of three-dimensional TFT arrays (col. 1) the stacking of TFT devices in three-dimensional arrays including a plurality of different vertical planar device levels 3A (or 2A) and 3B (or 2B)

(abstract and Figures 1 and 4) (col. 4, l. 30-39 and col. 6, l. 47-53); see also first and second planar layers 26 and 27 (col. 5, l. 55-65) in Figure 5A. *Combination* meets said claim limitations through

(1) a raised layer in the form of layer 2B (Figure 3 in Walker et al and col. 6, l. 54-63) in a region adjacent to any one of integrated circuit devices (TFTs) positioned at a lower level, such as 2A or 3A, with an upper surface of said raised layer (e.g., upper surface of 2B or 3B) being at a position higher than an upper surface of said integrated circuit (2A or 3A); and

(2) another semiconductor thin film bonded on the upper surface of said raised layer in the form of e.g. semiconductor film 13C (Figure 5A).

Motivation for inclusion of the teaching by Walker et al immediately flows from the reduction in cost through reduction in effective cell area by means of three-dimensional arrays (col. 1 in Walker).

The limitation "planarized" only has patentable weight in the device application of applicant to the extent the final structure is further limited by it. But "planarized" in "planarized region" (lines 4 and 6) does not add any patentable weight to the claim limitation, because whether a planarization step was carried out to render a structure planar is only a limitation on the method of making a structure. Even the process step of planarizing does not guarantee a planar surface, only an attempt to do so. A forteriori, then, a surface that has been illustrated as planar amply meets the claim limitation.

On claim 30-31: in the combined invention, with three-dimensional arrays of TFTs, the combined apparatus comprises further an electrically conductive layer (e.g the gate

layer 17 of a TFT positioned at a lower level; see e.g. Figures 1E and 2) is disposed between said semiconductor substrate and said semiconductor thin film (active layer of a TFT positioned at a level higher than said lower level) and also comprises further an interlayer dielectric layer disposed between said semiconductor substrate and said semiconductor thin film (namely: the specific interlayer dielectric layer such as 2A, 2B, ..., surrounding said gate layer 17).

3. ***Claim 16*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al as applied to claim 5, in view of Yamazaki et al (6,184,556 B1).

As detailed above, Zhang et al anticipate claim 5. Zhang et al do not necessarily teach said semiconductor thin film to be a compound semiconductor substrate as its main material. *However, SiGe, a compound semiconductor, has long been taught as preferable over silicon for its higher electron mobility, as witnessed by Yamazaki et al (see Third Embodiment, col. 15, l. 4-9). Motivation* for higher mobility of charge carriers is obvious because of the resulting faster response of the device. Moreover, it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. In re Leshin 125 USPQ 416.

4. ***Claim 20*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al as applied to claim 5, in view of Hayashi et al (JP-09045930 A).

As detailed above, Zhang et al anticipate claim 5. Zhang et al do not necessarily teach the further limitation as defined by claim 20. However, it would have been obvious to include said further limitation in view of Hayashi et al, who teach the application of

TFTs in active matrix displays for inter alia an optical printer head. It is thus seen that optical printer head applications are obvious applications of the active matrix display by Zhang et al. *Motivation* to include the teaching by Hayashi et al immediately flows from the resulting enlargement of the range of applications.

5. ***Claims 5, 9-10 and 26*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2003/0067043 A1) in view of Muto et al (JP 61102767 A).

Zhang teaches a combined semiconductor apparatus (three-dimensional IC memory array integrated with an embedded read-write memory (eRWM): title, abstract and [0023]-[0024]) comprising: a substrate having an integrated circuit (0s) ([0074]); a planar region (all regions below 23) formed in a surface of said substrate (Figures 9 and 10BA); and a semiconductor thin film (either 20a or 30a2: ([0109]) including at least one semiconductor device (P+/N-/N+ diode) and bonded on said planar region (Figure 10BA; in the case of 30a2 this bonding is indirect but present through 20a); and a planar film 23 (Figure 9A and [0101) disposed between said planar region and said semiconductor thin film.

The limitations "planarized" (lines 4 and 7) fail to further limit the planar region and planar film but instead only limit the method of making by describing a process step. Similarly, the limitation "wherein a surface of said planarized film on a side of said semiconductor thin film has been subjected to a planarizing process" does not further limit said planarized, i.e., planar, film so long as the planar surface of said planar film is on the side of the semiconductor device, which, as we have seen, is the case.

Zhang does not necessarily teach said substrate to be a semiconductor substrate. *However, as witnessed by Muto et al,* a compound semiconductor substrate of semi-insulating GaAs is advantageous because it allows read and write operations to be conducted at high speed (see English abstract). *Motivation,* to include the teaching by Muto et al, directly follows from the high read/write speed considering the eRWM component in the device by Zhang.

On claim 9: said semiconductor thin film as selected to be 30a2 has a common electrode layer 20a on a second surface of the semiconductor thin film opposed to a first surface of the semiconductor film, in which said semiconductor device is formed (first surface is upper main surface, second surface is lower main surface, of 30a2) (cf. Figure 10BA), and said second surface of said semiconductor thin film is disposed on a side of said planarized region of said semiconductor substrate (because said semiconductor substrate with planarized region is below said semiconductor thin film (cf. Figure 10BA).

On claim 10: said integrated circuit includes individual electrode terminals (source/drain terminal are inherent to the transistors 0T,...,(Figure 2A); said apparatus further comprising individual interconnecting lines 20av, 30av,.., formed on a region extending from an upper surface of said semiconductor device to said individual electrode terminals (cf. Figure 2A and [0074]).

On claim 26: because the integrated circuit comprises a three-dimensional memory array a raised layer such as 22" or 26 (Figures 9 and [010]) exists on any of the levels except the lowest one such that such raised layer in positioned (1) on a

surface of said semiconductor substrate as all other layers meet this claim limitation, (2) said raised layer is positioned in a region adjacent to said integrated circuit device (N.B.: any of the memory elements including those on the lowest level meet the claim limitation "integrated circuit device"), while, being at a level higher than the first level, said raised layer is at a position higher than an upper surface of said integrated circuit device that is at the lowest level (any of the memory cells at the lowest level). Another semiconductor thin film is bonded on 22" or 26.

6. ***Claims 27-28 and 33-34*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang et al and Walker et al as applied to claim 26, in view of Hayashi et al (JP-09045930 A).

*On claims 27 and 33:*As detailed above, Zhang et al anticipate claim 26. Zhang et al do not necessarily teach the further limitation as defined by claim 27. *However, it would have been obvious to include said further limitation in view of Hayashi et al*, who teach the application of TFTs in active matrix displays for inter alia an optical printer head. It is thus seen that optical printer head applications are obvious applications of the active matrix display by Zhang et al. *Motivation* to include the teaching by Hayashi et al immediately flows from the resulting enlargement of the range of applications.

On claims 28 and 34: in order to print an image of the printed symbol or figure inherently must be formed. The limitation "at least one optical print head" is met by "an optical print head", and therefore, the combination of the teaching by Hayashi et al also render claim 27 obvious for the same reasons as explained for claim 27.

1. ***Claim 32*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang and Muto et al as applied to claim 26 above, and further in view of Puar (4,342,102).

As detailed above, claim 26 is unpatentable over Zhang in view of Muto et al. Furthermore, said semiconductor thin film in Zhang includes a common electrode layer 20a ([0109]) on a second surface of said semiconductor thin film opposed to said first surface (namely on the other side than the one at which the semiconductor device is formed), and said integrated circuit has at least several source electrode terminals. Zhang does not necessarily teach said source electrode terminals to have a common voltage thus teaching the integrated circuit to have a common terminal. However, as evidenced by Puar in the art of memory arrays one common ground potential suffices for all source terminals (col. 2, l. 30-35). Motivation to include said teaching at least derives from the circumstance that voltages only have physical significance as differences and furthermore because the common ground potential saves additional cost otherwise needed top provide each source with a different voltage.

Double Patenting

A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

7. ***Claims 33-34*** are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 27-28. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Response to Arguments

Examiner regrets to have to change his opinion on patentability of the claimed subject matter of claim 5. However, planarization does not even guarantee a layer to have a planar surface, - only that a attempt has been made to make said layer more planar than it was, and thus any surface illustrated to be planar more than fulfils claim language. In addition, in light of this changed position the examiner has also included rejections based on new art, in particular Zhang et al and Walker et al as cited above, in addition to Hayashi et al and Yamazaki et al as cited above over which in addition to the repeated rejection over Zhang as cited in the previous office action the previous indication of allowable subject matter must be withdrawn.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Manning (4,900,693) (e.g., Figure 4 and cols. 1-5); and Ryou (5,492,851) as previously cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 24, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)